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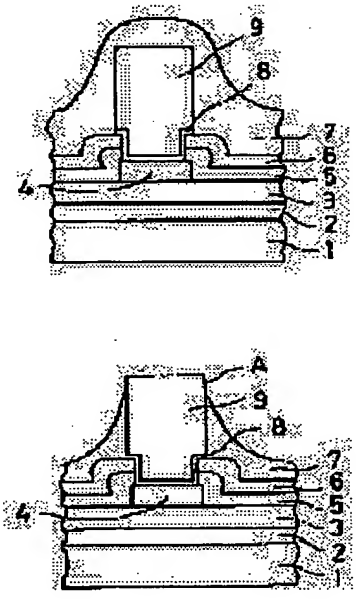
(54) FORMING METHOD FOR BUMP ELECTRODE

(57)Abstract:
PURPOSE: To provide a simple process and to improve reliability of a semiconductor element by covering an exposed part of a passivation layer and a polyimide layer for protecting a side of a bump electrode.
CONSTITUTION: A semiconductor substrate 1 is covered with insulator layers 2, 3, a pad layer 4 is superposed on the layers 2, 3, and passivation layers 5, 6 for burying the pad 4 are formed. Then, a bump electrode 9 having parts passing the layers 5, 6 to connect the pad 4 is formed, and a barrier metal layer 8 for covering the electrode 9 in contact with the layers 5, 6 is mounted. Then, it is covered with the exposed parts of the layers 5, 6 and a polyimide layer 7 for protecting the side of the electrode 9. For example, after a gold bump electrode 9 is mounted by a plating step, it is covered entirely with the layer 7, and then isotropically etched until an uppermost layer of the electrode 9 is observed.



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CLAIMS

[Claim(s)]

[Claim 1] The process which covers an insulating material layer to a semi-conductor substrate, and the process which piles up a pad layer at a part for said insulating material layer, The process which forms a bump electrode equipped with the part which connects with the process which forms the passivation layer which buries said pad, and said pad, and penetrates a passivation layer, The formation approach of the bump electrode characterized by providing the process which installs a wrap barrier metal layer for the bump electrode section which touches said passivation layer, and the process which puts the polyimide layer which protects the exposed part of said passivation layer, and the flank of a bump electrode

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] With respect to the approach of forming a polyimide layer in a semiconductor device, it carries out suitable [of this invention] to a bump electrode especially.

[0002]

[Description of the Prior Art] It changes also like an erector with improvement in the degree of integration of a semiconductor device, in addition to the method using a leadframe, the technique by the so-called bump electrode is used abundantly, and the present condition is that the improvement of a bump electrode is advanced.

[0003] the front face of the semi-conductor substrate 1 which consists, for example of silicon when the semiconductor device using a bump electrode is explained using drawing 1 -- the CVD (Chemical Vapour Depo-sition) layer 3 of NONDO-PU -- covering -- the part -- a conductive metal, for example, aluminum, or aluminum alloy A layer 2 and BPSG (Boro Phospho Silicate Glass) (from (aluminum-Si, aluminum-Si-Cu) -- the becoming pad layer 4 is formed.) This of connecting with the active element or passive element built to the semi-conductor substrate 1 electrically is

natural, and forms the bump electrode 9 in this in piles.

[0004] It is CVD although explanation gets mixed up. In a layer 2 and the BPSG layer 3, the double layer of the PSG (Phospho SilicateGlass) layer 5 and the silicon nitride layer 6 is covered. Since it is embedded in the passivation layer, into both contact part, the pad layer 4 which carries out the laminating of the metal bump electrode 9 forms the barrier metal layer 8, and it prevents a migration phenomenon etc. while utilizing the bump electrode 9 for fixing by plating. Moreover, a wrap will be in the metal bump electrode 9 and a connection condition about a passivation layer in the polyimide layer 7 (refer to drawing 1). In addition, while connecting an inner lead 10 to the bump electrode 9, in order to complete as a semiconductor device, the closure process by mold resin 11 is performed.

[0005] In addition, the polyimide layer 7 has covered neither the bump electrode 9 nor the barrier metal layer 8 so that clearly [drawing 1]. It is for the well-known photolithography technique's after covering the polyimide layer's 7 on the whole surface performing a patterning process in this, and forming puncturing in the polyimide layer 7. In addition, this process process extracts and explains main things, and writes that there are many skipped processes.

[0006] [Problem(s) to be Solved by the Invention] Thus, the well-known photolithography technique of using an aligner etc. on the occasion of formation of a bump electrode is indispensable, a process is complicated and, naturally a man day is also large compared with a process also with cost and considerable and the easy frequency which accident generates since it is complicated.

[0007] In addition, since the polyimide layer 7 is not covered by the bump electrode side attachment wall, it cannot be denied to it that the dependability as a semiconductor device falls. In addition, since it is covered with mold resin 11, an inner lead 10 and the metal bump electrode 9 are wrap PSG about the pad layer 4 as an ONARU passivation layer by the stress. A crack goes into the double layer of a layer 5 and the silicon nitride layer 6, and a defect occurs also in the wiring layer which follows the pad layer 4.

[0008] This invention was accomplished according to such a situation, and aims at offering the formation approach of the bump electrode by the simple process especially.

[0009] [Means for Solving the Problem] The process which covers an insulating material layer to a semi-conductor substrate, and the process which piles up a pad layer at a part for said insulating material layer, The process which forms a bump electrode equipped with the part

which connects with the process which forms the passivation layer which buries said pad layer, and said pad layer, and penetrates a passivation layer, There is the description of the formation approach of the bump electrode concerning this invention in the process which installs a wrap barrier metal layer for the bump electrode section which touches said passivation layer, and the process which puts the polyimide layer which protects the exposed part of said passivation layer, and the flank of a bump electrode.

[0010]

[Function] The polyimide film which covers with this invention the bump electrode which consists, for example of gold performs isotropic etching processing depended without an aligner until the top face of a bump electrode appears, it covers a side face with the polyimide film, and improves the dependability of a semiconductor device.

[0011] This invention which makes it a summary to process the bump electrode which consists of this gold until the top face of a bump electrode appears the wrap polyimide film on the occasion of performing isotropic etching based on knowledge that removal of the polyimide film of a flank is rather difficult was completed.

[0012]

[Example] The example concerning this invention is explained with reference to drawing 2 thru/or drawing 5 . The passive element or the active element is formed in the semi-conductor substrate 1 of the first conductivity type which forms the bump electrode concerning this invention which consists of silicon with the conventional method, and it is CVD in the front face. The film 2 and the BPSG film 3 are covered (refer to drawing 2).

[0013] Preparing aluminum or the electrode made from aluminum alloy (aluminum-Si, aluminum-Si-Cu) which changes from a conductive metal layer to said active element and passive element, and a wiring layer (neither is illustrated) on the other hand, a wiring layer forms semi-conductor substrate 1 front face on a wrap insulating material layer.

[0014] It is CVD so that it may be made clear to drawing 1 . In a layer 2 and the BPSG layer 3, it is PSG. The double layer of a layer 5 and the silicon nitride layer 6 is covered. Namely, CVD Although the pad electrode 4 made from aluminum or aluminum alloy (aluminum-Si, aluminum-Si-Cu) is formed in the layered product of the film 2 and the BPSG film 3 according to the patterning process using the well-known photolithography method, magnitude is usually 80-micrometer square from 100-micrometer square.

[0015] PSG whose thickness is 0.4 micrometers in order to prevent the effect from moisture ONARU which consists of a layer 5 and the silicon nitride layer 6 whose thickness is 0.75 micrometers (On aluminum) According to the deposition

process of a passivation layer, i.e., an insulating material layer Although the pad electrode 4 is embedded, succeedingly, according to the patterning process by the well-known photolithography method same with formation of the pad electrode 4, the aperture 12 which removes a wrap deposit part for the pad electrode 4, and penetrates a passivation layer is formed, and pad electrode 4 front face is exposed. In the flank of pad electrode 4 front face exposed to the aperture 12, and a passivation layer, the barrier metal layer 8 is formed, and while using the golden bump electrode 13 for fixing at a plating process, migration etc. is prevented.

[0016] As a barrier metal layer 8, it will consider as titanium, nickel, and the three-tiered structure of PARAJUUMU, the bump electrode 9 of gold will be used as an electrode for plating process fixing according to a plating process, and both will be in the successive state.

[0017] According to the magnitude of the pad electrode 4, the width of face of the bump electrode 9 of gold writes in addition what is written to width of face and reverse in each drawing, although height is about 18 micrometers.

[0018] Thus, the polyimide layer 7 is covered over the whole and the cross-section structure of drawing 2 takes after installing the bump electrode 9 of gold. Next, although isotropic etching processing is performed until the maximum upper layer of the bump electrode 9 of gold can be seen, etching time is beforehand decided with the dummy of the same conditions. By this processing, the bump electrode 9 of gold which the polyimide layer 7 put on **** A is formed, and it shifts to degree process.

[0019] As degree process, it changes from copper or a copper alloy to the bump electrode 9 of gold, and width of face fixes the inner lead 10 whose 30-40-micrometer thickness is about 35 micrometers according to a bonding process, closes the resin layer 11 for the whole by the transfermold method further, and completes a plastic molded type semiconductor device (refer to drawing 4).

[0020]

[Effect of the Invention]

1. By such formation approach of a bump electrode, a production process is simplified and it is that the cost is cut down.

[0021] 2. There is an advantage which can be covered completely conversely without a flank's being able to remove the bump electrode of gold very much by etching of a wrap polyimide layer. For this reason, compared with the conventional product, the very advantageous heat cycle test result was obtained. This was shown in the curvilinear Fig. of drawing 5 . That is, when a percent defective is taken on an axis of ordinate and a cycle is taken on an axis of abscissa, this invention article of

the trigonum mark and outstanding ****** of single or more figures are seen in 300 or 500 cycles, and, as for the conventional article of a round mark, the effectiveness of this invention is clear. This shows that the stress by closure resin is eased.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the important section of the conventional plastic molded type semiconductor device.

[Drawing 2] It is the sectional view showing the production process back of the plastic molded type semiconductor device concerning this invention.

[Drawing 3] It is the sectional view of the plastic molded type semiconductor device obtained according to the process after drawing 2.

[Drawing 4] It is the sectional view of the plastic molded type semiconductor device obtained according to the process after drawing 3.

[Drawing 5] It is the curvilinear Fig. showing the property of elegance the plastic molded type semiconductor device concerning this invention, and conventionally.

[Description of Notations]

1: Semi-conductor substrate,
2: CVD Layer,
3: BPSG layer,
4: Pad electrode,
5: PSG Layer,
6: Silicon nitride layer,
7: Polyimide layer,
8: Barrier metal layer,
9: Bump electrode,
10: Inner lead,
11: Closure resin layer.